Application Number: 09/841,536
Application Filed: 04/24/2001
Applicant: Sanjay Agarwal, Sapna Agrawal
Title: Coprocessor architecture for control processors using synchronous logic.
Examiner: Pan, Daniel H

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May 3rd, 2004.

To:
Commissioner for Patents
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Sir:

In response to the office action mailed 03/05/04, please consider the following responses:

a) With reference to item 5: Shackleford et al. method of register file use is different with respect to the method described in my invention. It would not be possible to anticipate my method with reference to Shakleford et al. (5,896,521). Please refer to the detailed explanation in item b.
b) With reference to item 6: Shakleford et al. describes [col. 9, lines 52-54] using data input selector **242** as a mechanism for controlling the selection of four sources that are inputs to the register file. The data input selector controls which functional output is being fed into the register file system. The data selector input **242** in Shakeleford et al. describes how the instruction word is used to select the operands [col. 9, lines 54-67]. The data input selector **242** is not used to select the math operation itself.

   The invention described in my patent application and claim 2 refers to selecting the math operation itself using 8-bit register as an interface as described in FIG. 13. Fields M1, M0, and SLSR are used to select the required math function.

Considering the above facts, I wanted to request USPTO to consider claim 2 as a valid claim and process this patent application accordingly.

Sincerely,
S Agarwal
(Sanjay Agarwal)

S Agrawal
(Sapna Agrawal)